The Effect of Negative Feedback on Single Event Transient Propagation in Digital Circuits

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Abstract—Propagation and attenuation of Single Event Transient (SET) pulses in combinational logic circuits are examined. A Miller feedback mechanism that affects the minimum pulse width needed for SET propagation in combinational logic circuits is identified. Analytical models that are commonly employed to predict the combinational Soft Error Rate (SER) of future integrated circuit (IC) technologies do not include this feedback effect. Inclusion of this effect increases the critical charge required for SET propagation through a combinational logic circuit by more than 30%. This feedback phenomenon reduces the estimated SER, which is sensitive to changes in critical charge, by more than 40%.

Index Terms—Single Event, SET, Soft Error, feedback, SER, critical charge, Miller effect

I. INTRODUCTION

With ever-decreasing minimum dimensions of integrated circuits (ICs), accompanied by higher operating frequencies, lower supply voltages, and lower noise margins, the sensitivity of circuits to single event transient (SET) pulses increases significantly [1–3]. For CMOS ICs, an energetic particle strike can cause a transient voltage perturbation, called a single event transient (SET), that propagates through the circuit and may become stored as incorrect data, causing disruption of the circuit operation. Upset rates due to SETs are dependent on the pulse width of the SET and the clock frequency. With increasing clock frequency there are more latching clock edges to capture an SET. With decreasing feature sizes the charge required to represent a logic HIGH state decreases, resulting in an increased number of SETs. For advanced technologies, the errors due to SETs are expected to dominate the overall error rate of the entire circuit [2]. One major factor that determines the error rate for combinational circuits is SET pulse width [2].

CMOS logic gates typically act as low pass filters for an SET pulse. Thus, an SET pulse is not able to propagate through a chain of logic gates without attenuation unless the pulse is longer than some minimum value. Because the vulnerability of a circuit is determined by the shortest SET pulse that can propagate through it, this paper focuses on SET pulses of very short duration as compared to normal circuit signals. As discussed in [4], transients wider than the transition time of an individual gate propagate without any attenuation through a series of similar gates. Mavis et al. have studied the critical pulse width for propagation through an infinitely long chain of inverters without attenuation, as a function of technology node [5].

In this work, propagation and attenuation of SET pulses is examined using detailed models and circuit simulations. A significant increase in the critical pulse width required for propagation is observed when we include the effects of negative feedback between logic gates.

Predictions of combinational-logic soft error rates (SERs) in future IC technology nodes are commonly made using analytical models, as precise SPICE-like models are unavailable for processes still under development [6]. Fig. 1 is an example of such SER estimation as a function of technology node [6]. The combinational logic SER in Fig. 1 has been plotted for different pipeline depths (or clock period in number of fan-out-4 (FO-4) delays). The curves indicate an increase in SER with decreasing clock period. Such combinational logic SER trend is usually computed by taking...
into account the various masking effects on the SETs, such as electrical masking, latch-window masking and logical masking [6, 7]. The electrical masking is computed using the Horowitz rise and fall time model [8] along with the delay degradation effect [9] (or other similar models). However, these models typically do not include the effects of cell-level negative feedback during switching events.

Capacitive coupling between the input and output of a CMOS inverter affects both the inverter itself and the load of the inverter, which increases the duration of the switching transition. These effects are described in detail in Section II. In this work, we show that this negative feedback between the output and input of each CMOS gate increases the minimum pulse width needed for propagation. This mechanism is important in assessing the reliability of digital circuits and for accurately predicting error rates in combinational logic circuits for future technologies. This paper presents an analysis of this feedback effect for 250 nm to 130 nm CMOS technologies. The feedback effect increases the critical pulse width required for propagation through combinational logic circuits, reducing the estimated error rate when compared to techniques that do not take the negative feedback into account.

In this work, the feedback mechanism is analyzed using SPICE based circuit simulations and an analytical model is presented for this effect. The impacts of this effect on the critical charge and SER are also presented. The rest of the paper is organized as follows. Section II describes capacitive coupling in digital circuits and discusses the causes for the negative feedback. Section III provides an analysis of the feedback effect and presents an analytical model. Simulation results for gate transition times, critical charge and SER are presented in section IV. Section V summarizes the impact of the feedback phenomenon.

II. COUPLING EFFECT IN DIGITAL CIRCUITS

In CMOS ICs, any node making a logic transition can act as an aggressor net, injecting charge into neighboring nets termed as victims. Fig 2(a) depicts a classic example of a

![Crosstalk model](image1)

Fig. 2 (a) Crosstalk model [10] and (b) coupling between two series connected inverters

![Capacitive coupling](image2)

Fig. 3 (a) Schematic of a series of 10 inverters with (b) simulations showing the transitions of outputs 8, 9 and 10.
crosstalk model [10] in which capacitive coupling between signal lines can degrade digital signal integrity. Similar coupling effects within individual gates (output-to-input and input-to-output, Fig. 2(b)) are evident in a SPICE simulation of a string of inverters as shown in Fig. 3. The overshoot and undershoot at the output of each gate is caused by each inverter’s intrinsic input-to-output coupling capacitance (due to the gate-to-drain capacitances of the transistors) during switching. For example, when the output of the eighth inverter (O8) begins switching from low-to-high, the output of the ninth inverter (O9) overshoots as the output voltage of O8 is coupled to the output of O9 via its gate-to-drain capacitance before O9 begins switching from high-to-low. These over/undershoot effects are readily observed in SPICE simulations and are important due to their potential to trigger latchup in CMOS circuits [11].

In addition to under/overshoot, a second coupling effect can also be observed during switching transitions. As each inverter completes its output transition, the load inverter (i.e., the next inverter in the path) is also transitioning in the opposite direction. Thus, the effective load capacitance is dynamically modulated by the Miller input capacitance of the load inverter and the load inverter presents a net larger capacitance to the previous inverter than it would without the Miller effect. In contrast to the input-to-output coupling of under/overshoot, this output-to-input coupling generates negative feedback that slows the final transition of each gate. For example, consider the high-to-low output voltage transition of inverter O8 over the period of 420 ps to 480 ps in Fig. 3(b). The slope between 450 ps to 480 ps is clearly much less steep than the slope from 420 ps to 450 ps as the negative feedback from O9 to O8 slows the transition. In contrast, over the period from 470 ps to 500 ps the high-to-low output voltage of the final stage (O10) shows no such effect since it does not have another logic gate as load (even though it has the same static load capacitance).

Another effect of this negative feedback mechanism can be observed if pulse widths are compared as the Cgd feedback elements are varied. Modified Level 1 SPICE models were used to isolate and illustrate this effect in a chain of 80 inverters. Although this is a longer logic chain than would occur in practical integrated circuits, it is useful for illustrating the phenomenon. The coupling between inverter stages was varied by changing the ratio of feedback capacitance (Cgd) to load capacitance (CL) for each inverter while keeping the total capacitance (Cgd+CL) constant. Pulse width was measured at half the maximum voltage swing (VDD/2). Fig. 4 shows the SET pulse width at the output of each inverter after a 90 ps SET pulse was introduced at the input of the first inverter. These simulations demonstrate that the width of the pulse decreases as the pulse proceeds along the inverter chain. Furthermore, as the feedback capacitance increases relative to the total output capacitance (resulting in increased negative feedback between adjacent inverters), the SET pulse width degrades more rapidly.

In fact, given sufficiently high feedback and a sufficiently long chain of CMOS gates, any SET pulse will eventually decay in a combinational logic circuit. This result may seem counterintuitive, as the active signal regeneration of each logic gate might be expected to force a signal to propagate endlessly through an inverter chain of infinite length. However, these simulation results clearly indicate that negative feedback effects must be considered in the SET analysis to improve the accuracy of timing predictions. The physical phenomena responsible for this result are discussed in the following section.

III. AN ANALYSIS OF THE EFFECT OF FEEDBACK ON GATE OUTPUT CAPACITANCE

As stated earlier, analytical models such as the Horowitz rise and fall time model [8] have been commonly used for assessing the performance of a combinational logic gate and for computing technology trends in SER. Such models compute the transition time of a gate in terms of RC time delays assuming a fixed value of capacitance. A gate in a combinational logic circuit is modeled using the drain-to-source resistance (rds) of individual transistors along with the load capacitance (CL) seen by the gate. Simple analysis
indicates that the transition time also significantly depends on the dynamic feedback capacitance of the loading gate(s). The driving gate, in addition to driving its intrinsic load capacitance, must also drive the gate-to-drain capacitance (\( C_{gd} \)) of the loading gate(s). Thus a weaker driving gate (greater \( r_{ds} \)) or a greater \( C_{gd} \) will directly result in an increase in the transition time needed to charge or discharge the gate output. The effective load capacitance depends heavily on the Miller gain effect on \( C_{gd} \) with a maximum during the transition period when both the PMOS and NMOS transistors are ON and the gate behaves like a linear amplifier.

A simple analytical model can be used to quantify the Miller effect of the gate-to-drain capacitance (\( C_{gd} \)) on the output voltage of a logic gate (Fig. 5). The driving logic gate is modeled as a Thévenin voltage source in series with an effective resistance and output capacitance. We start with the assumption that the output of the driving inverter is transitioning from low-to-high. (The case of a high-to-low transition will lead to a similar result.) Neglecting the contribution of the NMOS transistor, the inverter can be modeled as an equivalent PMOS drain-to-source resistance (\( r_{ds} \)) and output capacitance (\( C_L \)). During the transition phase, the second (load) inverter is modeled as an amplifier with an inverting gain of \( -A \) and a coupling capacitance (\( C_{gd} \)) between input and output as shown in Fig. 5.

By nodal analysis,

\[
\frac{V_{in} - V_G}{r_{ds}} = \frac{V_G - V_{out}}{sC_L} + \frac{V_G}{sC_{gd}}.
\]

(1)

Substituting \( V_{out} = -AV_G \) and rearranging terms yields the following expression for the transfer function \( V_G / V_{in} \):

\[
\frac{V_G}{V_{in}} = \frac{1}{1 + s \times r_{ds} \times (C_L + (1 + A) \times C_{gd})}.
\]

(2)

From this transfer function the dependence of the gain on the product of \( r_{ds} \times (C_L + C_{gd}) \) is clear. Feedback from the following stage causes an additional term proportional to \( A \times r_{ds} \times C_{gd} \) to increase the effective RC time constant of the prior stage, increasing its transition time and making it less responsive to pulses of short duration. (The Miller effect also results in an increased capacitance at the output of the inverter stage, but the reflected capacitance on the output of the stage is divided by the gain instead of multiplied, and hence is negligible.) This analysis is an example of Miller Effect capacitive multiplication that analog circuit designers are already familiar with, except that in this case it only occurs over the portion of the switching curve where the inverter behaves like a high gain amplifier. Although the gain magnitude \( A \) is only significant over a portion of the output transition, its effect is still sufficient to increase gate transition time significantly and attenuate SET pulse width.

To illustrate the Miller effect on the load capacitance, an ac simulation was performed on an inverter to obtain its input capacitance vs. gate voltage characteristics. Simulations were conducted using the Cadence circuit simulation tool Spectre [12]. The IBM 0.13-µm technology was chosen for the simulations, and Spectre models generated by the IBM process design kit (PDK) were used throughout the 130 nm study. Figure 6 clearly indicates the Miller effect on the input capacitance of the inverter. The input capacitance is not fixed, but is gain multiplied and reaches a peak during switching which is about 6 times its nominal value.

IV. PULSE ATTENUATION AND GATE TRANSITION TIMES

The attenuation of transient pulses of varying widths was studied using a relatively long chain of fan-out-1 (FO-1) inverters. An SET pulse that does not propagate through FO-1 minimum sized inverters will not be able to propagate through a chain of any other CMOS gate. Thus FO-1 inverters are commonly used to define the critical transient width needed for a given technology [5]. The Spectre simulations were conducted using IBM 0.13-µm technology. The inverters were
sized appropriately to obtain equal rise and fall times.

The transition time measured for a single inverter stage with a passive load capacitance (approximately equal to the input capacitance of an inverter stage) was approximately 70 ps. This value increased to approximately 100 ps when an active inverter stage was used as the load. Figure 7 shows a plot of pulse width as a function of the inverter stage number. Although an 80 ps pulse eventually died out at the 90th stage, a 120 ps pulse was able to propagate without significant attenuation over 150 inverter stages.

Figure 8 is a plot of the critical transient width needed for infinite propagation vs. feature size. In addition to the IBM 0.13-µm technology, TSMC 0.18-µm, 0.25-µm and 0.4-µm technologies and Spectre models generated by their respective PDKs were used to obtain this plot. As stated earlier, our estimates indicate a significant shift in the plot from earlier predictions [5] that did not include the feedback phenomenon described here. Our simulations indicate that SET pulses lower than this critical width will propagate a finite distance with attenuation that depends on the specific pulse width.

Error rates in a more realistic combinatorial logic path, typically limited to about 10 stages of logic between latches or I/O’s, will depend on the extent of attenuation. The greater the attenuation, the greater will be the probability of latch window masking effects. Error rate computations must therefore take the feedback effect into account for more realistic predictions.

The critical charge required to upset a node in a chain of FO-4 inverters was also studied. The analysis was initially carried out using a fixed load capacitance without the presence of the active feedback loading effect. This model is similar to some of the analytical models that have been used earlier for SER predictions [6]. Next, the simulations were repeated taking into account the effect of Miller capacitance loading due to the gate-to-drain capacitance of the load inverter. Figure 9 is a plot of critical charge as a function of the technology node for the two cases considered above. The results indicate that the critical charge increases by more than 30% when the feedback effect is taken into account and that this increase is independent of the technology node.

Hazucha and Svensson recently developed a model for SER estimation in CMOS SRAM circuits [13], as given in Equation (3). Since combinational and memory elements are constructed from the same basic devices, this model was extended to estimating combinational SER in [6].

$$SER \propto F \times A \times \exp \left( -\frac{Q_{\text{crit}}}{Q_{S}} \right)$$

where

- $F$ is the flux with energy $> 1$ MeV, in particles/(cm\(^2\times\)s),
- $A$ is the area of the circuit sensitive to particle strikes, in cm\(^2\),
- $Q_{\text{crit}}$ is the critical charge, in fC, and
- $Q_{S}$ is a charge collection parameter for the device, in fC.

$Q_{S}$ is a measure of the charge generated by a particle strike. From Equation 3 it is clear that the estimated SER is very sensitive to relative changes in $Q_{\text{crit}}$ with respect to $Q_{S}$. Figure 10 is a plot of $\exp(-Q_{\text{crit}}/Q_{S})$, which is directly proportional to the SER, as a function of technology for the cases with and without Cgd.

![Fig. 8. Critical transient width for infinite SET pulse propagation vs. feature size.](image1)

![Fig. 9. Critical charge for infinite SET pulse propagation vs. feature size.](image2)

![Fig. 10. Variation of soft error rate (which is proportional to $\exp(-Q_{\text{crit}}/Q_{S})$) vs. feature size.](image3)
without the Miller capacitance loading effect. When the feedback effect is taken into account, the SER is reduced by about 40% for the 0.13 µm technology and by about 90% for the 0.25 µm technology. The reduction in the percent change in SER for advanced technologies is attributed to the fact that \( Q_{\text{crit}} \) scales more rapidly than \( Q_s \) and is of the order of \( Q_s \). Thus, relative changes in \( Q_{\text{crit}} \) to \( Q_s \) are not magnified by the exponent term; instead the SER is approximately proportional to \( 1/Q_{\text{crit}} \). These results indicate that the reduction in the estimated SER will be significant even for advanced technologies and the Miller feedback effect must be included for more accurate combinational SER predictions.

V. CONCLUSION

In addition to well-known over/undershoot effects, Miller effect has been identified to affect transient pulse propagation in digital circuits through load capacitance modification and increase in transition time of a logic gate. An analytical approach has been used to describe the effect. Simulations indicate that the minimum pulse width required for propagation through an infinitely long chain of inverters in a 0.13-µm technology is of the order of 100 ps, which is significantly higher than previously reported values [5]. Critical charge for SET propagation through a combinational logic chain increases by more than 30% and the corresponding SER decreases by over 40% when this effect is included. The mechanism identified in this work can appreciably affect error rate computations in digital ICs and should be incorporated in analytical models used for error rate predictions of future technologies.

REFERENCES