

# On-Chip Characterization of Single-Event Transient Pulsewidths

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**Abstract**—A new on-chip single-event transient (SET) test structure has been developed to autonomously characterize the widths of random SET pulses. Simulation results show measurement granularity of 900 ps for a 1.5  $\mu\text{m}$  technology and also indicate that the measurement granularity rapidly scales down with technology. Laser tests were used to demonstrate circuit operation on test chips fabricated using a 1.5  $\mu\text{m}$  process. The experimental results indicate pulsewidths varying from about 900 ps to over 3 ns as the laser energy was increased.

**Index Terms**—CMOS, radiation hardening by design (RHBD), single event, single-event transient (SET), single event upset (SEU), transient pulsewidth.

## I. INTRODUCTION

CHARACTERIZATION of radiation-induced single-event transients (SETs), which are temporary perturbations initiated in logic gates, in commercial digital ICs has become more critical as clock speeds have increased and feature sizes have decreased in modern IC processes [1]. With each new technology node, submicrometer ICs have become more vulnerable to charge deposited directly by alpha particle strikes or indirectly by terrestrial neutron strikes [2]. An energetic particle strike in a CMOS IC can cause a transient voltage perturbation that propagates through the circuit and becomes latched as incorrect data, potentially resulting in data corruption or system failure. Consequently, SET-induced soft errors have now become a significant reliability concern in ground-based commercial and consumer electronics.

Previous work has shown that errors due to SETs increase linearly with clock frequency [3]. Fig. 1 shows the relative contribution to error rates for combinational and sequential logic as a function of frequency [3]. At higher frequencies, or for advanced technologies, the error rates for combinational logic begin to dominate [3]–[6]. This phenomenon can be explained by the increased number of clock edges for latching SETs and the lower charge needed to represent a logic HIGH state (resulting in a higher number of SETs) [4]. Recent work

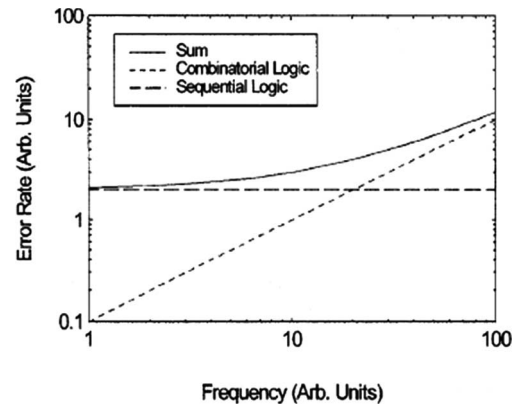


Fig. 1. Error rates in combinational and sequential logic as a function of frequency (after [2]).

suggests that for 0.25  $\mu\text{m}$  and smaller technologies, SETs in combinational logic will dominate single-event-related reliability issues [7].

The probability that an SET will result in an error is dependent on the propagation distance through the combinational logic circuit and the arrival time of the SET at the latch input [1], [8]. The width of a transient voltage pulse is determined by many factors, including the nature of the ionizing particle, the linear energy transfer of the particle, the circuit characteristics, the technology used, the location of the strike, and the incident angle of the strike [1], [9]–[13]. Wider pulses have a greater probability of being present at the latching edge of the clock. Thus, characterizing the widths of transient voltage pulses is of paramount importance in the prediction and mitigation of single-event effects for an advanced technology.

The characterization of SET pulses has been accomplished with a variety of techniques in prior research. In some cases, the transient current pulses that are responsible for initiating SETs have been measured directly using oscilloscopes [14]–[17]. However, such direct off-chip measurements are difficult to perform because of pulse distortion due to the stray capacitances of the measurement system (i.e., loading and line capacitance effects).

Other researchers have characterized voltage pulsewidths as transients propagate through logic gates using multiple latches with delayed signal paths [13] and/or delayed clock signals. The advantage of this approach is that the delay can be continuously varied. However, multiple identical hits are needed while the

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delay is matched to the transient pulsewidth. Another technique is the use of a chain of identical cells that are monitored by latches to characterize the pulsewidth in terms of multiples of the individual cell delay [18]. In this approach, the latches are clocked continuously to obtain information about the state of the cells. However, due to limitations of the maximum clock frequency that can be applied, it can be difficult to capture a very fast SET pulse using this method.

In this paper, we describe a new SET test circuit that can complement the techniques previously described. This test circuit can characterize the width of SET voltage pulses as they propagate through logic gates without the need for an external trigger or multiple laser strikes. The basic principle of operation of this circuit is similar to the one proposed in [18] but incorporates a *self-triggering* mechanism that does not require an outside timing signal to indicate the occurrence of an SET pulse. This test structure captures the SET pulse in a series of latches, which can be easily read out to determine the width of the pulse. This circuit technique can be used in CMOS, BiCMOS, and silicon-on-insulator processes, regardless of feature size or operating speed.

## II. AUTONOMOUS PULSEWIDTH CHARACTERIZATION

### A. Pulse Capture Circuit

A basic unit for elapsed time in a digital IC is the propagation delay associated with an inverter, designated as one inverter delay. The test circuit described here characterizes the SET pulsewidth in units of inverter delays. Pulsewidth is defined as the width of the pulse measured at the inverter threshold ( $V_{dd}/2$ ). If an SET pulse of sufficient duration is input to an inverter chain, it will propagate through each inverter after a specific time delay (e.g., it will reach the third inverter after two inverter delays, it will reach the fifth inverter after four inverter delays, and so on). This is shown in Fig. 2, where the leading edge of the transient pulse is shown to reach the inputs of inverters in a chain at different instances of time. As time progresses, this transient propagates through a series of inverters. Thus, at any instant, a certain number of inverters will have their outputs affected/switched. This number of affected inverters is proportional to the transient pulsewidth. For extremely short pulse durations, the pulse becomes attenuated as it propagates through logic gates. As discussed in [19], pulses wider than the logic transition time of a gate will propagate through the gate without attenuation, whereas pulses shorter than the transition time will propagate with varying attenuation. For each technology, simulation results showed that the minimum pulse duration (measured at the inverter threshold of  $V_{dd}/2$ ) for propagation through multiple levels of logic is approximately equal to the delay of the logic gate in that technology. Simulations also showed that pulse shaping has a negligible effect on the pulsewidth when the width of the pulse is greater than the transition time of the logic gate.

The approach outlined here is most effective for measuring transient pulsewidths that are greater than the threshold for propagation through the test circuit. However, in a combinational logic path that is limited to about ten stages of logic, SETs generated close to the receivers contribute the most to

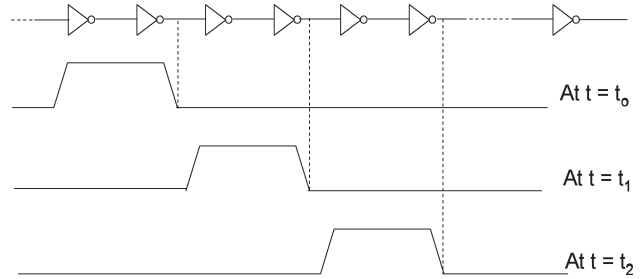


Fig. 2. Pulse propagation through a series of inverters. Time instances  $t_0$ ,  $t_1$ , and  $t_2$  are two inverter delays apart.

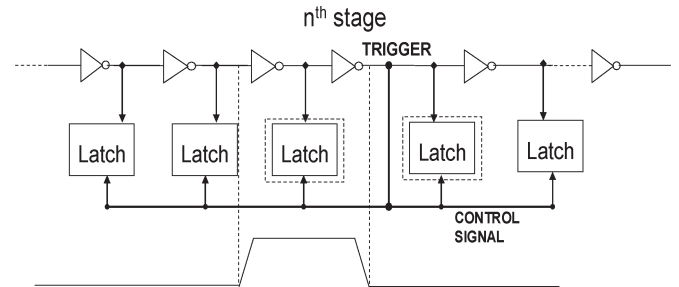


Fig. 3. Output of the  $n$ th stage can be used to provide hold signal for latches to freeze the data and the SET pulse.

combinational soft error rate (SER). In short logic paths, SETs that are slightly shorter than the length required for indefinite propagation may also contribute to the total SER. These short pulses will not be measured by this approach.

Fig. 2 illustrates an example of pulse propagation through a series of inverters when the SET pulse is two inverter delays long. The pulse will affect two inverter outputs as it propagates through the chain. If the number of such inverters whose outputs are affected by the SET pulse can be determined at any instant, the pulsewidth can be estimated as a multiple of inverter delays. Simulations showed that for all pulsewidths between  $[(n - 0.5) \times \text{stage delay}]$  to  $[(n + 0.5) \times \text{stage delay}]$ , the number of affected stages is  $n$ . Thus, the pulsewidth determined will be accurate to within  $\pm$  one-half of the stage delay.

To capture the affected outputs from a chain of inverters, the output of every inverter is connected to an asynchronous latch as shown in Fig. 3. As the SET pulse propagates through an inverter, the data stored in its respective latch will change. However, once the SET pulse passes, the inverter output and latch data will revert to their original states. (Note that the additional loading due to the latch at the inverter output will alter the pulse characteristics. Hence, capacitance at the latch input must be minimized and accounted for when determining the inverter delay for accurate measurement of pulsewidth.) If the latches are placed in a *hold* mode while the SET pulse is within the inverter chain, each latch will retain the logic state of its respective inverter.

For laser tests, the exact instant when the hit takes place is known, and the latches can be placed on *hold* after a certain delay such that the SET pulse is guaranteed to be present within the inverter chain. However, for heavy ion testing, information regarding the hit time and hit node is usually not available. To address autonomous operation in such cases, the output of one

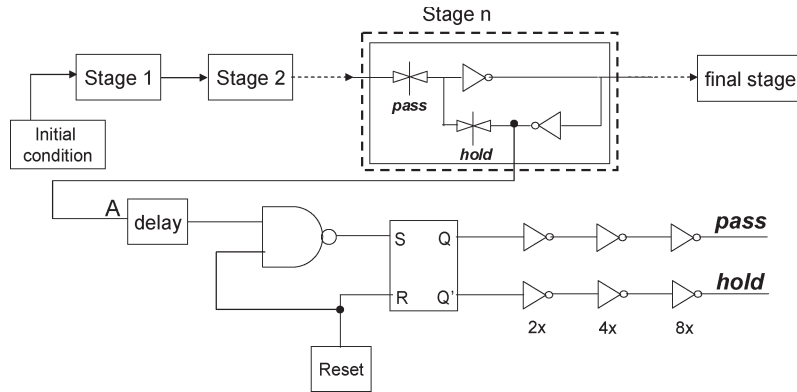


Fig. 4. Test structure showing individual stages along with the trigger/reset circuit. Highlighted region shows the internal circuitry of individual stages.

of the inverter stages can be used as a trigger signal. To make this circuit *self-triggering*, a transition at the output of the  $n$ th stage (or trigger stage) can be used to trigger the latches to hold the states of the inverters as shown in Fig. 3. As the output of the  $n$ th stage triggers the *hold* signal internally, precise information regarding the hit time (or location) is unnecessary. Note that a hit on any stage past the trigger stage does not affect the trigger stage output. Thus, to latch an SET pulse, a hit must take place on a stage before the trigger stage.

The instant when the SET pulse is latched, the initial hit stage may or may not have recovered to its original state. The initial stage will not recover to its original state if the charge collection is not completed when the SET pulse is latched. If the initial stage has recovered fully when the pulse is latched, the pulsewidth measured is the actual pulsewidth (to within the accuracy of one inverter delay). However, if the initial stage has not recovered, it is possible that the charge collection still continues, and the actual pulsewidth could be longer than the measured width. For laser tests, the initial hit stage can be precisely targeted, but for heavy ion tests, the hit stage is not identifiable, and hence, it cannot be ascertained whether the hit stage has fully recovered or not. To address this uncertainty, a delay can be introduced in the trigger signal, and extra inverter stages can be added beyond the trigger stage to allow the complete SET pulse to propagate well past the trigger stage before latching occurs. The distance that the SET pulse travels along the inverter chain will be proportional to the trigger signal delay, which should be equal to the maximum SET pulsewidth expected during measurement. If the complete SET pulse has moved beyond the trigger stage, one can safely assume that the estimated pulsewidth is the actual pulsewidth (to within a resolution of one inverter delay), irrespective of the hit node.

Based on this approach, a test circuit was designed and evaluated. To simplify the circuit and reduce loading effects, the individual inverter stages were implemented using the inverting outputs of standard CMOS passgate latches, as shown in Fig. 4. The logic transition time of each inverting latch stage was found to be approximately 2.5 times the transition time of an individual inverter in this technology. Thus, SET pulses wider than 2.5 times the transition time of an inverter could be resolved and measured. Since this particular circuit was intended strictly for laser testing, the number of latches past the trigger stage could be kept to a minimum.

The operation of the test circuit is straightforward. During the SET-propagate phase, the *pass* signal is ON, and the *hold* signal is OFF. As a result, each inverter output is connected to the next stage, allowing the SET pulse to propagate through the inverters and passgates. When the leading edge of the SET pulse reaches the  $n$ th stage, it triggers an SR flip-flop, which subsequently turns off all passgates by inverting the *pass* signal and freezing the data in the latches by turning on the *hold* signal. The SET pulsewidth is directly proportional to the number of latches whose output is affected. Once the latch outputs have been read out, a *reset* signal is used to initialize the *pass* and *hold* signals and make the circuit ready for measuring the next pulse.

The latches used in our test circuit were not hardened since this circuit was strictly intended for laser testing. In the case of alpha/neutron or heavy-ion testing, the probability of upsetting the latch and the probability for inducing an SET in the circuit are dependent on the circuit area. Depending on the design, upsets in latch circuits may dominate SETs generated in the combinational circuit. Hence, for a circuit intended for such testing, one option is to use latches that are hardened by design. The other option would be use of regular unhardened latches along with an ion collector (e.g., a huge array of inverters) that feeds into the pulse capture circuit. In this case, the probability of latch upset would be much lower than creating an SET. In addition, since SET pulses greater than the transition time of an inverter will propagate without attenuation [19], most SETs propagating through the ion collector do not get attenuated, and the measurement is not affected.

Finally, for most cases, a latch upset can clearly be identified by looking at the data pattern (when the latch that is upset is not the first or the last latch that contains the data). Such spurious data can then be discarded. For advanced technology designs that utilize a large number of latches (since the delay of an inverter stage gets smaller as technology advances), the percentage error in the measurement will be sufficiently low to provide an acceptable estimate of the pulsewidth.

### III. SIMULATION AND EXPERIMENTAL RESULTS

To provide a proof of concept, a test chip was designed and fabricated to demonstrate the validity of this approach. The design was simulated with the Cadence Spectre simulator

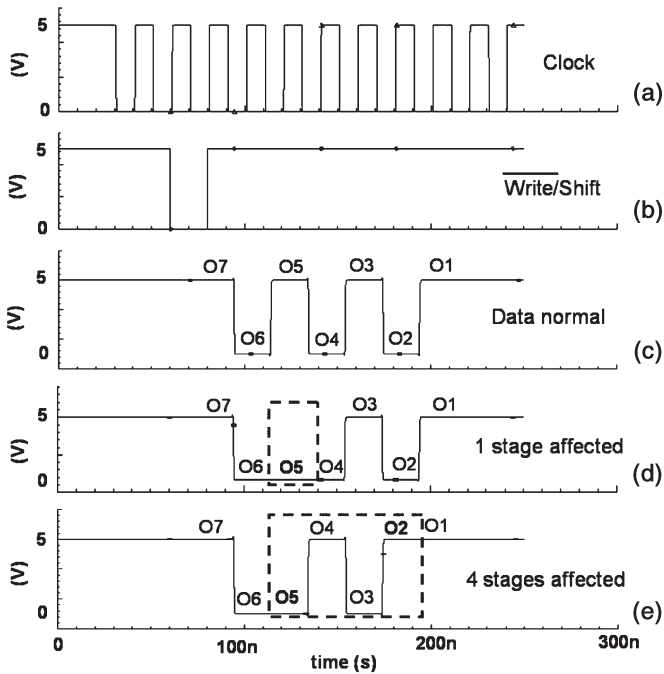


Fig. 5. Waveforms showing (a) clock to the data shift register, (b) write/shift control signal to the data shift register, (c) output of data shift register prior to an SET strike, (d) output with a 1.2-ns SET pulse, indicating that one stage has a switched state, and (e) output with a 3.85-ns SET pulse, indicating that four stages have switched states.

[20] and fabricated using the AMI 1.5  $\mu\text{m}$  process available through MOSIS ([www.mosis.org](http://www.mosis.org)). During the simulations and the actual measurements, the input to the first inverter in the chain was held low, thereby setting the outputs of odd stages high and the outputs of even stages low. The third stage was used to generate the trigger signal, which, in turn, was fed to the SR flip-flop. If a strike occurred in the first or second stage, it would generate an SET pulse that would propagate through the third stage and trigger the SR flip-flop to change its state. Note that the propagation delays of the SR flip-flop and its output buffers would permit the leading edge of the SET pulse to travel beyond the third stage before latching occurred. As a result, additional inverters (and associated latches) were added beyond the third stage. The leading edge of any SET pulse was found to be latched at the fifth stage. To reduce the number of I/O pins, a data shift register was included to read the outputs of the latches serially.

An SET timing analysis was performed for the test circuit using AMI 1.5  $\mu\text{m}$  MOSFET models. Simulation results showed that the delay of an individual inverter/latch stage for the 1.5  $\mu\text{m}$  technology was approximately 900 ps. With five stages, the test circuit could, therefore, characterize SET pulsewidths in increments of 900 ps up to a maximum value of 4.5 ns. As stated earlier, the measurements would be accurate to within  $\pm$  one-half the delay of an individual stage or  $\pm 450$  ps for the 1.5  $\mu\text{m}$  technology.

Fig. 5 shows the simulation results for the output of the data shift register before and after an SET. A double-exponential current source was used to model SET charge injection at the output of the first stage. The amount of collected charge,

and, thus, the width of the generated SET pulse, was varied by adjusting the amplitude of the current source. For each measurement cycle, the actual SET pulsewidth created at the current injection node was compared to the number of latch stages with flipped output states in order to determine the accuracy of the pulsewidth estimates.

Fig. 5(a) shows the clock signal used to output the latch data serially. Fig. 5(b) shows the write control signal to the data shift register. When the write control signal goes low, the current state of every stage in the pulse capture circuit is stored in the data shift register; when the signal is high, the data are serially shifted out. Fig. 5(c) shows the serial latch data in the absence of an SET pulse. Fig. 5(d) shows the latch data with an actual SET pulsewidth of 1.2 ns. In this case, only the fifth stage is affected by the SET, as evidenced by the inverter values read out in Fig. 5(c). Fig. 5(e) shows the latch data for a longer SET pulse of 3.85 ns. As can be seen, the number of stages affected by the SET is four (second through fifth). Thus, for the first case (short pulse), the pulsewidth is estimated to lie between 0.45 and 1.35 ns (i.e.,  $900 \pm 450$  ps). For the second case in which four latches have switched states, the pulsewidth is estimated to lie between 3.15 and 4.05 ns (i.e.,  $3.6 \pm 450$  ps). In both cases, the SET pulsewidth measured at the current injection node lies well within these estimates.

Laser tests were performed on these test chips at the U.S. Naval Research Laboratory, using a standard laser test procedure previously described in the literature [21], [22]. In this procedure, the collected charge as well as the SET pulsewidth is varied by adjusting the laser pulse energy. A good correlation between ion and laser data for the collected charge has been reported using this technique [22], thereby validating the use of laser tests to determine the single-event sensitivity of devices.

Fig. 6 shows a die photograph of the 1.5  $\mu\text{m}$  technology test chip. The laser pulse energy was varied from 85 to 179 pJ. The second stage of the test circuit chain, which is highlighted in Fig. 6, was used as the laser target.

Fig. 7 shows the experimental results of the output of the data shift register before and after the laser strikes on the second stage. These results correlated very well with the simulated results in Fig. 5. For an 85-pJ laser pulse, only one stage switched its state (stage 5) as seen in Fig. 7(b). This result corresponded to an SET pulsewidth between 0.45 and 1.35 ns. As the hit node had fully recovered in this case, the actual pulsewidth was, therefore, known to be within the captured pulsewidth range. As the laser pulse energy increased, the number of switched states also increased. Laser energies between 85 and 179 pJ resulted in one, two, or three stages being affected. These results all showed that the hit node had recovered fully and that the actual pulsewidth was within 900 ps times the number of stages,  $\pm 450$  ps.

At laser pulse energies of 179 pJ and above, four stages switched states as shown in Fig. 7. However, in these cases, the hit node did not fully recover, and the pulsewidth could no longer be accurately determined. However, longer pulsewidths at higher energies could easily have been characterized if the test circuit has included additional stages and a longer trigger delay to allow the hit stage to fully recover. Overall, these results provide a proof of concept that such on-chip

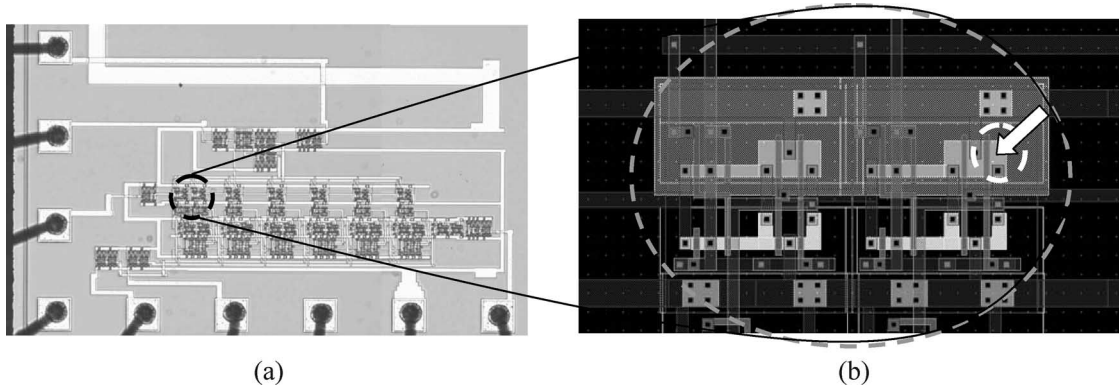


Fig. 6. (a) Die photo of 1.5  $\mu\text{m}$  technology test chip. (b) Zoom-in picture that indicates the strike location on the layout.

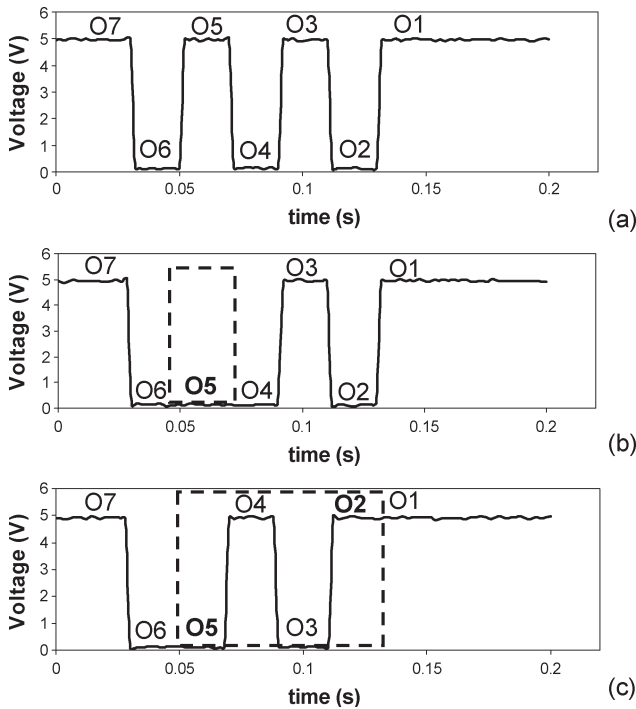


Fig. 7. Waveforms showing (a) output of data shift register prior to a laser strike, (b) with 85 pJ pulse energy, and (c) with 179 pJ pulse energy. With a lower laser pulse energy, one stage has a switched state, whereas for the higher laser pulse energy, four stages have switched states (outlined regions).

characterization circuits can be used effectively to determine SET pulsewidths.

#### IV. EXTENSION TO ADVANCED TECHNOLOGIES

Clearly, the granularity associated with the relatively long inverter delay of the AMI 1.5  $\mu\text{m}$  technology limited the resolution of the measured pulsewidths. However, since gate propagation delay decreases as feature size decreases, the SET width resolution was expected to dramatically improve in more advanced submicrometer IC processes.

As stated in [23], the time scale of charge collection could range anywhere between a few picoseconds and a few hundred picoseconds. However, these times for collection of charge are not necessarily that of the resulting voltage pulse. The voltage pulse characteristics will be influenced by the device

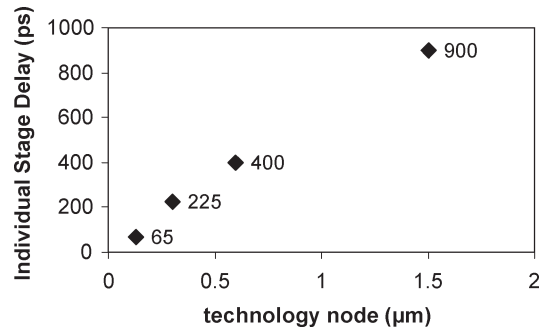


Fig. 8. Individual stage delay as a function of the technology.

drive currents, nodal capacitance, and the collected charge. For advanced technologies, such a voltage pulse could become comparable to the delay of a single inverter stage or even larger than that. Thus, as the delay of a single inverter decreases with advances in technology, the accuracy of the measurement will continue to improve. To ensure that the charge collection has been completed (i.e., hit node has returned to its original voltage value and, thus, ensures that the voltage pulsewidth measured is that of the *actual* voltage pulse, accounting for both the prompt and delayed charge collection), it is necessary to allow the voltage pulse to propagate a few more stages beyond the trigger stage by increasing the number of stages and the delay in the trigger signal, as pointed out earlier. This allows the charge collection to be completed and the entire SET pulse to propagate past the trigger stage.

To confirm the hypothesis of improved measurement resolution, simulations of this measurement concept were carried out for the HP 0.6  $\mu\text{m}$ , TSMC 0.3  $\mu\text{m}$ , and IBM 0.13  $\mu\text{m}$  technologies. For each of these technologies, the basic circuit design remained the same, except that the device sizes were scaled appropriately. As expected, the delay for individual stages decreased as the minimum feature size decreased. Fig. 8 shows how the minimum pulsewidth as well as the related measurement resolution scales with technology. For the 1.5  $\mu\text{m}$  technology, the resolution of the pulsewidth measurement was 900 ps. This resolution decreased to 400, 225, and 65 ps for the 0.6, 0.3, and 0.13  $\mu\text{m}$  technologies, respectively. Only the simulation results for the 0.13  $\mu\text{m}$  process are discussed in detail, since the 0.6 and 0.3  $\mu\text{m}$  technologies showed similar results.

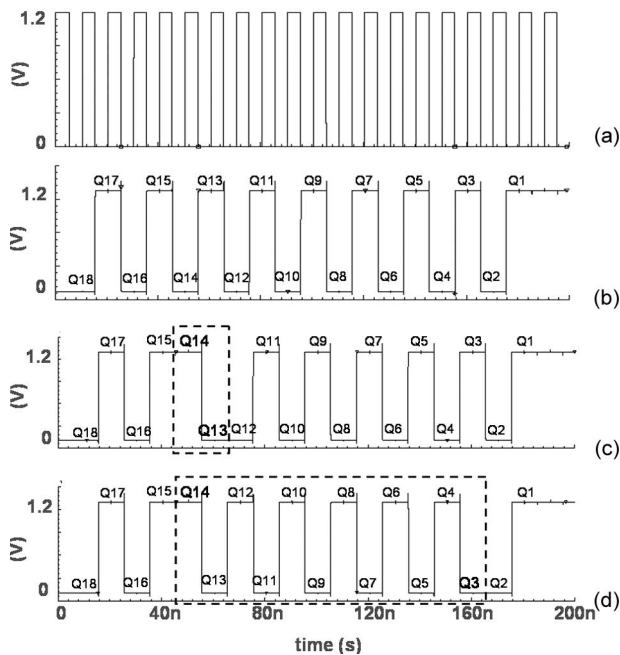


Fig. 9. Waveforms showing (a) clock to data shift register, (b) output of data shift register without any SET, (c) output with a short SET, and (d) output with a wide SET. For the short SET, two stages have switched states, and for the wide pulse, 12 stages have switched states (outlined regions).

Simulation results showed that the delay of an individual inverter in the  $0.13\ \mu\text{m}$  process was 25 ps. However, when this inverter output was loaded by the other latch components, the minimum delay increased to approximately 65 ps. Due to the reduced resolution, a total of 18 series-connected latch stages were used in the  $0.13\ \mu\text{m}$  test circuit simulation.

Fig. 9 shows the simulation results for the output of the data shift register prior to and after an SET. A double-exponential current source was once again used to simulate charge injection at the output of the second stage. The trigger signal was taken from the output of the eleventh stage. Fig. 9(a) shows the clock signal used to output the latch data serially. Fig. 9(b) shows the serial latch data in the absence of an SET pulse. Fig. 9(c) shows the latch data for a short SET pulse. In this case, the outputs of the thirteenth and fourteenth stages are affected by the SET, as evidenced by the inverter values when compared to Fig. 9(b). Fig. 9(d) shows the latch data for a long SET pulse, where 12 stages (third through fourteenth) are affected. Thus, for the first case (short-duration pulse), the pulsewidth is estimated to lie between 97.5 and 162.5 ps ( $65\ \text{ps} \times 2 = 130 \pm 32.5\ \text{ps}$ ). For the second case (long-duration pulse), the SET pulsewidth is estimated to lie between 747.5 and 812.5 ps ( $65\ \text{ps} \times 12 = 780 \pm 32.5\ \text{ps}$ ). From the simulation, the pulsewidths created by the current source were found to equal 160 and 770 ps, respectively, once again confirming that the actual pulsewidths lie within the range estimates calculated by reading the latch outputs.

Note that in both simulations, the hit node fully recovered before the SET pulse was latched, thereby ensuring that the pulsewidth was accurately captured. Furthermore, a relatively small delay was used in the trigger signal to reduce the number of stages in the simulation, resulting in the capture of the SET

pulse on either side of trigger stage. If the design were to be used for heavy ion tests, a longer delay would be required in the trigger stage to ensure that the entire SET pulse has traveled past the trigger stage before latching occurred. In this case, additional stages would be added past the trigger stage to ensure that the complete SET pulse was captured.

## V. CONCLUSION

A new self-triggered test structure for measuring SET pulsewidth in increments of one inverter delay has been described. Simulation results from four different IC technologies and experimental results from test chips fabricated in a  $1.5\ \mu\text{m}$  technology validate the use of this method to characterize transient pulsewidths. Simulation results show measurement resolution of 900 ps for a  $1.5\ \mu\text{m}$  process, scaling to a 65-ps resolution for a  $0.13\ \mu\text{m}$  process. Experimental pulsewidth measurements from the  $1.5\text{-}\mu\text{m}$  test chip indicated pulsewidths varying from 900 ps to over 3 ns as the laser energy at the strike location increased from 85 to 179 pJ. Longer inverter chains would permit the capture of even longer pulsewidth, whereas decreased feature sizes (and inverter propagation delays) would improve the resolution of this technique even further. This pulsewidth measurement technique readily scales with decreasing feature sizes in commercial IC processes and can provide a simple yet straightforward method for characterizing SETs that may lead to soft errors in high-performance digital systems.

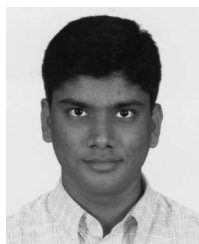
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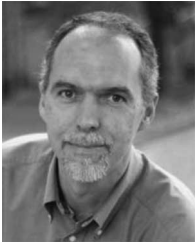
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