Integrated Diagnostic/Prognostic Experimental Setup for Capacitor Degradation and Health Monitoring

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***Abstract*—This paper proposes the experiments and setups for studying diagnosis and prognosis of electrolytic capacitors in DC-DC power converters. Electrolytic capacitors and power MOSFET's have higher failure rates than other components in DC-DC converter systems. Currently, our work focuses on experimental analysis and modeling electrolytic capacitors degradation and its effects on the output of DC-DC converter systems. The output degradation is typically measured by the increase in Equivalent series resistance and decrease in capacitance leading to output ripple currents.Typically, the ripple current effects dominate, and they can have adverse effects on downstream components. A model based approach to studying degradation phenomena enables us to combine the physics based modeling of the DC-DC converter with physics of failure models of capacitor degradation, and predict using stochastic simulation methods how system performance deteriorates with time. Degradation experiments were conducted where electrolytic capacitors were subjected to electrical and thermal stress to accelerate the aging of the system. This more systematic analysis may provide a more general and accurate method for computing the remaining useful life (RUL) of the component and the converter system.**

I. Introduction

In DC-DC converter power supply hardware electrolytic capacitors and MOSFET's have higher failure and degradation rates than other components in the systems. Variety of factors, such as High Voltage conditions, Operating Temperature, Transients, Reverse Bias, Strong Vibrations and high ripple current attribute to the failure in these components. These degraded units affect the performance and efficiency of the DC-DC converters in a significant way. Degradation and failures in the components occurs due to prolong operation periods under normal conditions or operations under extreme stress conditions like high temperature and high voltage. The paper develops a method for studying the degradation effects of electrolytic capacitors subjected to loading under extreme operating conditions i.e. high voltage stress and observe their impact on overall system performance.

Switched-mode power supplies are widely used in DC-DC converters because of their high efficiency and compact size. They have an very significant application use in portable electronic devices, which derive their power primarily from batteries. Such electronic devices often contain several sub-circuits with different voltage requirements (sometimes higher and sometimes lower than the supply voltage, and possibly even negative voltage). DC-DC converters can provide additional functionality for boosting the battery voltage as the battery charge declines. A typical buck-boost DC-DC converter schematic circuit is illustrated in Fig. 1.

In the literature it has been reported that electrolytic capacitors are the leading cause for breakdowns in power supply systems [1], [2]. The performance of the electrolytic capacitor is strongly affected by its operating conditions, which includes voltage, current, frequency, and working temperature. For degraded electrolytic capacitor the impedance path for the ac current in the output filter keeps increasing, thus introducing a ripple voltage on top of the desired DC voltage [3]. Continued degradation of the capacitor leads the converter output voltage to also drop below specifications and in some cases the combined effects of the voltage drop and the ripples may damage the converter itself in addition to affecting downstream components.

The degradation in the DC-DC converters is typically measured by the increase in ESR (Equivalent Series Resistance) and decrease in capacitance value which leads to high ripple current and the drop in output voltage at the load. Typically the ripple current effects dominate, and they can have adverse effects on downstream components. The work in this paper is specifically directed towards DC-DC converters in Avionics systems [4]. In these systems the power supply drives a GPS unit, and ripple currents at the converter output can cause glitches in the GPS position and velocity output, and this, in turn, may cause errors in the Inertial Navigation (INAV) system causing the aircraft to fly off course [5].

In general, capacitor degradation has been studied under nominal conditions as well as under extreme stress conditions, such as high voltage, high ripple, and adverse thermal conditions [6], [7]. Our overall goal in this work is to perform a systematic study of capacitor degradation stress conditions by replicating and extending some of the experimental studies that have been carried out in the past. Our approach is to

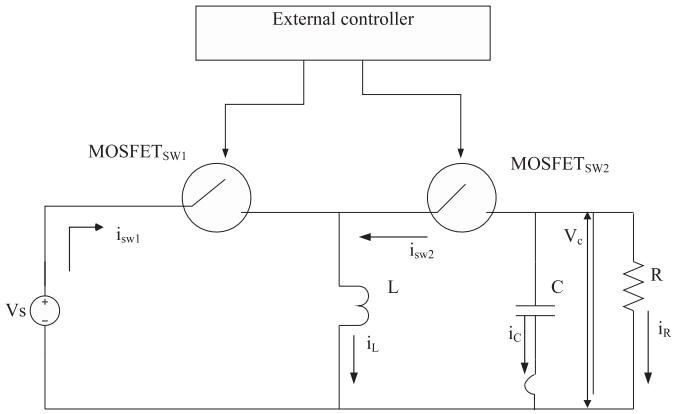

Fig. 1. Buck Boost converter Schematic Circuit(Ref [6])

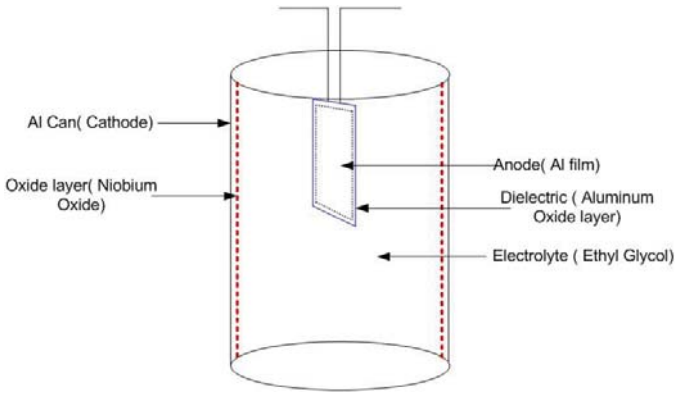

Fig. 2. Physical Model of Electrolytic Capacitor (Ref [6])

perform empirical studies and then link them to theoretically-derived physics of failure models. This paper presents a first step by systematically collecting accelerated capacitor degradation data at high voltage operation. The results are observed, analyzed and are further compared with data observed from degradation under normal operating conditions. We also discuss and present our preliminary work for capacitance degradation in this paper as a first step to studying capacitance degradation using physics of failure models. The experimental studies, conducted at the NASA Ames Prognostics Centre of Excellence Lab, are discussed in greater detail along with observed result analysis later in the paper.

The rest of this paper is organized as follows. The following section discusses the capacitor model and mechanisms for capacitor degradation in DC-DC converters. The next section discusses accelerated degradation experiments conducted on electrolytic capacitors under high voltage stress. The following sections discusses preliminary results for the experimental setup and the analysis of the collected data. The paper concludes with discussion of the results and future work.

II. ELECTROLYTIC CAPACITOR DEGRADATION

This section discusses in detail the conditions under which the capacitor degrades leading to faults in the system. We study the adverse effects of the load conditions, operating conditions, ripple currents, which cause degradation by raising the temperatures in the capacitor core.

A. Physical Model of the Capacitor

An aluminum electrolytic capacitor, illustrated in Fig. 2 consists of a cathode aluminum foil, electrolytic paper, electrolyte, and an aluminum oxide layer on the anode foil surface, which acts as the dielectric. When in contact with the electrolyte, the oxide layer possesses an excellent forward direction insulation property [8]. Together with magnified effective surface area attained by etching the foil, a high capacitance is obtained in a small volume [9].

Since the oxide layer has rectifying properties, a capacitor has polarity. If both the anode and cathode foils have an oxide layer, the capacitors would be bipolar [10]. In this paper, we analyze the "non-solid" aluminum electrolytic capacitors in which the electrolytic paper is impregnated with liquid electrolyte. There is another type of aluminum electrolytic capacitor, that uses solid electrolyte but we will not include these types of capacitors in this discussion [11].

B. Degradation Mechanisms

There are several factors that cause degradation in electrolytic capacitors. Over the period of time as the degradation increases the component finally fails , and this impacts the overall system functionality. The definition of failure and some of the failure modes are discussed below. Failures in a capacitor can be one of two types: (1) catastrophic failures, where there is complete loss of functionality due to a short or open circuit, and (2) degradation failures, where there is gradual deterioration of capacitor function. Degradations are linked to an increase in the equivalent series resistance (ESR) and decrease in capacitance over time [12], [13]. Capacitor degradation is typically attributed to:

1) High Voltage conditions: The capacitance decreases and ESR increases.
2) Transients: The leakage current can be high and an internal short-circuits can occur.
3) Reverse Bias: The leakage current becomes high with loss of capacitance and increase in ESR.
4) Strong Vibrations: These can cause internal short circuits, capacitance losses, high leakage currents, increase in ESR and open circuits.
5) High Ripple current: These cause internal heating, increasing the core temperature which results in gradual aging of the capacitor.

C. AGEING METHOD

In prognostic analysis we predict the behavior of the component using condition based monitoring. Under normal operating conditions the device lasts for several years and the

process of condition based monitoring becomes difficult. So study the systematic degradation of the component in shorter period of time is simulated under possible operating conditions. In these experimental setups the devices are subjected to higher stressors like high voltage, temperature etc which degrade the device significantly in a shorter period of time. Using condition based monitoring we can then characterize the device at regular intervals. If tasked properly then tests can give us failure targeted to a particular failure. This data from regular monitoring can then be used for prognostic algorithms for calculating the RUL under certain operating conditions. Thus by simulating certain accelerated conditions and monitoring the degradation systematically can be used for prognostic studies.

Presently in our study we can focussing our goal towards studying the degradation in electrolytic capacitors. A primary reason for wear out in aluminum electrolytic capacitors is due to vaporization of electrolyte, which, in turn leads to a drift in the main electrical parameters of the capacitor. One of the primary parameters is the equivalent series resistance (ESR). The ESR of the capacitor is the sum of the resistance due to aluminum oxide, electrolyte, spacer, and electrodes (foil, tabbing, leads, and ohmic contacts)[7], [8]. The health of the capacitor is often measured by the ESR value. Over the operating period, the capacitor degrades, i.e., its capacitance decreases and ESR increases. Considering the current ESR value and operating conditions the remaining useful life of the capacitor can be calculated using model-based methods. There are certain industry standards for these parameter values, if the measurements exceed these standards then the component is considered failed, i.e., the component has reached its end of life, and should be immediately replaced before further operations [1], [14], [15]. The next section discusses in detail the experiments being conducted on the electrolytic capacitors to study and measure the degradation the relevant capacitor parameters.

III. HARDWARE IMPLEMENTATION

For this experiment six capacitors in a set were considered for each varying electrical stress setup. Electrolytic capacitors of 2200μF capacitance, with a maximum rated voltage of 10V, maximum current rating of 1A and maximum operating temperature of 105°C was used for the study. These were the recommended capacitors by the manufacturer for DC-DC converters. The capacitors used for the experiments were picked from the same lot of one manufacturer, and all the capacitors in the lot had similar specifications. The electrolytic capacitors under test were characterized in detail before the start of the experiment at room temperature.

Since in this experiment we are studying the effect of high voltage on degradation of the capacitors, the capacitors were subjected to high voltage stress through an external supply source using a specially developed hardware. Fig. 3 shows the block diagram of the setup for the electrical stress experiment. The details of each of the instruments and specific hardware used in the experiment is discussed as below.

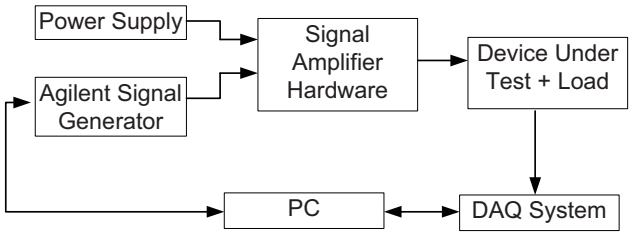

Fig. 3. Block Diagram of the Experimental Setup

A. Power Supply

The power supply used for the experiment is a BK Precession 1761 triple output DC power supply. A constant DC voltage of $\pm$15V is required by the amplification hardware which is provided by this power supply.

B. Function Generator

In the experiment we are charging/discharging the capacitors are a fixed frequency using a square wave input. This input square wave is generated using a Agilent 33220A 20 MHz Function/Arbitrary Waveform Generator. This is a 14-bit, 50 MSa/s, 64 k-point arbitrary waveforms generator and can be controlled over USB, GPIB and LAN

The function generator is programmed for a 1V square wave output at 200mHz. This frequency is calculated depending upon the RC time constant where R is the load connected for the capacitor to discharge and C the capacitance values of the capacitor. At this frequency the capacitor charges and discharges completely.

C. Amplification Stage

The manufacturer rates the capacitor at maximum 10V operating voltage. To observe the degradation due to electrical charge/discharge stress on the capacitor we stress the capacitors are different voltages specifically 8V, 10V, 12V and 15V.

To generate these different voltage levels from the function generator for a same square wave input we have developed a specific hardware as shown in Fig. 4. Opamp 7171 IC's are used in the inverting amplification mode with varying gains to obtain the required square wave voltages.

D. Load Resistor

To discharge the capacitor completely before the next charging cycle a resistive load was connected. The load selected is calculated such that the capacitor is completely discharged before the next charge cycle at 200mHz and the load should be able to sink sufficient amount of current to dissipate enough power. From these calculation a 1W 100Ω resistor was selected as a load.

E. Measurements Done on the hardware

In the charing/discharging cycle initially the capacitors charge/discharge simultaneously but as time progress and the capacitors degrade the charge/dicharge time varies for each capacitor. Though the capacitors are subjected to similar conditions their ESR and capacitance values change and this

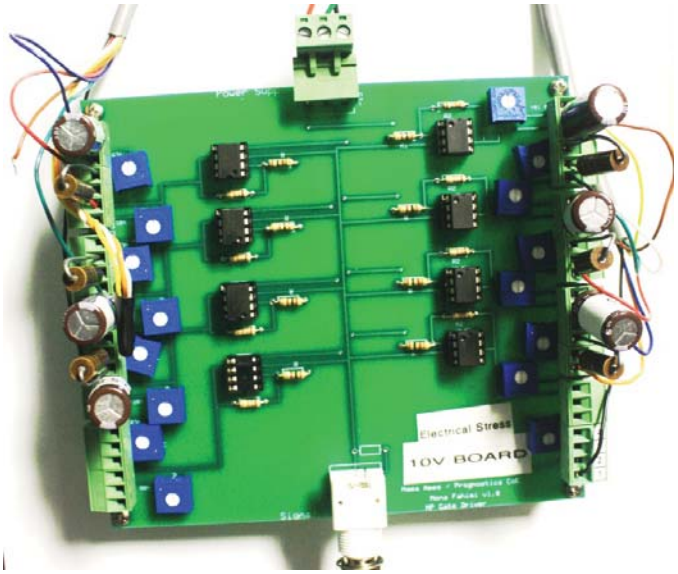

Fig. 4. Custom Module PCB developed for Signal Amplifier Hardware

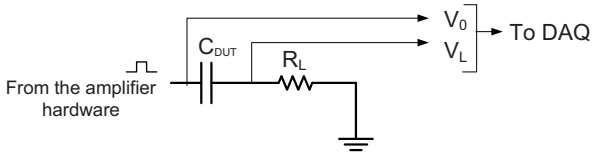

Fig. 5. Schematic for the Data Acquisition Signals

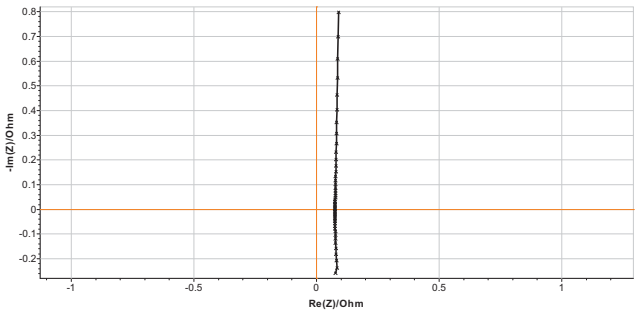

Fig. 6. Initial Characterization Plot

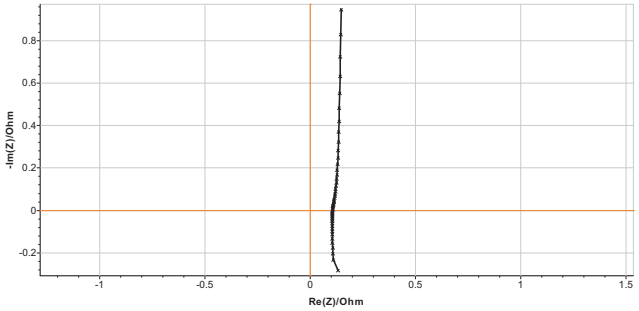

Fig. 7. Characterization Plot after 120 hours

affects the RC- time constant during charge/discharge. To monitor this charging/discharging of each capacitor under test we measure the input and output voltages of the capacitor.

Due to the charging/ discharging cycle the internal temperature of the capacitor increases. To monitor the rise in the temperature, a temperature sensor was connected to the bare aluminium part on the top of the can. Along with this measurement we also monitored the ambient room temperature in which the experiment was conducted. The schematic shown in Fig. 5 shows the measurements taken for each capacitor.

F. Impedance measurement

As discussed earlier ESR and capacitance are the two parameters on which the health of the capacitors is based upon. To characterize the capacitors we use a Impedance Measurement instrument.

The Electrochemical Impedance spectroscopy (EIS) finds many applications in corrosion, battery, fuel cell development, sensors and physical electrochemistry. It can provide information on reaction parameters, corrosion rates, electrode surfaces porosity, coating, mass transport, interfacial capacitance. Impedance measurements can be made in a potentiostatic mode (PEIS) or in a galvanostatic mode (GEIS).

The PEIS mode is used for characterizing all the capacitors under test. PEIS experiment performs impedance measurements into potentiostatic mode by adding a small sinusoidal voltage to a DC potential that can be set to a fixed value or relatively to the cell equilibrium potential. The equation of the working electrode versus time is:

$$E_{WE}(t) = E_{WE} + V_a sin(2\pi ft) \quad (1)$$

with Va the potential amplitude and f the frequency.

The ESR value is the real impedance measured through the terminal software of the instrument. Similarly the capacitance value is computed from the imaginary impedance using Electrochemical Impedance (EIS) Spectroscopy Z-Fit. The details of the method are in [16], [17]. These values can be calculated directly at the time of measurement or later off-line. Figure 6 shows the plot for real impedance Vs imaginary impedance for a pristine capacitor. The real impedance indicates the ESR value while the capacitance is calculated from the imaginary impedance value. Using the EIS Z-fit analysis it can be seen that the plot is almost a straight line indicating that the initial parameters are not degraded.

In Fig. 7 we observe deviations in the plot at the end of 120 hours of operation. This indicates that the ESR and capacitance have changed due to electrical stress applied during the operation.

G. Data Acquisition

The measurements discussed above are recorded using a National Instruments data acquisition hardware. A PXI 1033 M Series Multifunction DAQ chassis is used. This is a low-cost chassis for remote control applications, controlled from a PCI Express Card laptop host. The PXI-Express remote

controller achieves up to 110 MB/s sustained throughput. The chassis accepts up to 5 peripheral modules, we are presently using 3 modules for the experiment. Accepts both 3U PXI and Compact PCI modules.

NI PXI-6221 with 16-Bit, 250 kS/s, 16 Analog Inputs Two 16-bit analog outputs (833 kS/s, 24 digital I/O, 32-bit counters, is used as one of the peripheral modules for data acquisition. The voltage pins, temperature sensors wiring is connected to the SCC-68 Board which in turn is connected to the PXI-6221 module.

The NI SCC-68 is provided with SCC Expansion Slots I/O connector block . The connection block features 68 screw terminals for I/O signal connection, and power bus terminals for external power and grounding. The SCC-68 has four SCC slots for integrating thermocouple and for other signals. 68 screw terminals for easy I/O connections 4 expansion slots for analog input and digital I/O SCC signal conditioning modules are provided. The terminal block is provided with 16 analog input channels to which the voltage measurements are connected. Built-in cold-junction compensation for low-cost thermocouple measurements

A SCC-TC02 module used for temperature measurement connected to the slots provided on the SCC-68. SCC-TC02 are single-input modules for conditioning signals from a variety of thermocouple types, including T type thermocouple (which we are using for capacitor temperature measurement in the experiments) and millivolt inputs with a range of ± 100 mV. The NI SCC-TC modules include a 2 Hz lowpass filter, an instrumentation amplifier with a gain of 100, and buffered outputs for maximum scanning rates by the multifunction DAQ device. The SCC-TC modules include an onboard thermistor for cold-junction compensation.

Figure 8 shows the complete setup for the experiment excluding the characterization EIS instrument. The ESR and capacitance values were measured using an SP-150 Biologic SAS measuring instrument. The average initial ESR value was measured to be around 0.0758 mΩ and average capacitance of 1757μF for the set of capacitors under test. The degrading electrolytic capacitor is modelled as a series RC circuit.

A constant voltage source with a square wave of 200 mHz frequency and 1V output was used for generating the required signal. The output voltage from the source was then ramped upto the different voltage levels using the amplification hardware. A load of 100 Ω as discussed earlier was connected at capacitor terminal to discharge the capacitor completely within the specified cycle time. A GUI has been developed to monitor the charge/discharge voltage using the Lab View provided by NI. Figure 9 shows the screen shot of the front end of the GUI. The 4 different plots in the GUI show the charge/discharge wave form, current waveform (the current is calculated for each capacitor after characterizing and measuring the ESR which is updated periodically), voltage across the capacitor and finally the room and capacitor can top temperature.

Figure 10 shows the plots for the same measurements at the end of 120 hours of operation. At the end of this time it is observed from the charge/discharge that the capacitors

Fig. 8. Actual Experimental Setup

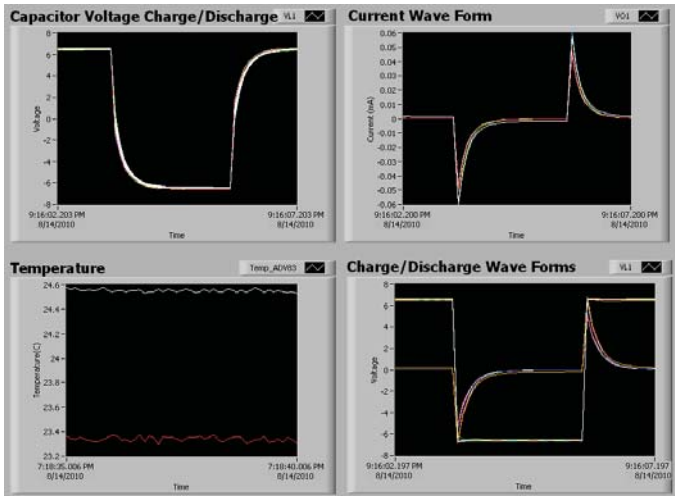

Fig. 9. Plots of the capacitor set signals at Start Time

have degraded differently as we can see a difference in the charge/discharge waveforms. With the change in the ESR and capacitance the RC-time constant changes as seen in the plot. These values are also recorded at the back-end in a txt file which can be later used for the data analysis.

IV. PRELIMINARY RESULTS

With the setup discussed above we carried out 100 plus hours of initial runs on the capacitors under different conditions. The preliminary results for both the increase in the ESR and decrease in the capacitance under these conditions are as shown in the tables.

The same set of capacitors were subjected to varying stress voltage for specified period of time. The details of test is show in the table I. The table shows the increase in the ESR over the period of 120 hours of operation. The capacitor is rated for 10V as per the manufacturer specification. In the experiment we applied voltage below the rated voltage and above the rated to study the degradation process on the capacitors. It can be seen that the rate of increase in the ESR varies as the stress

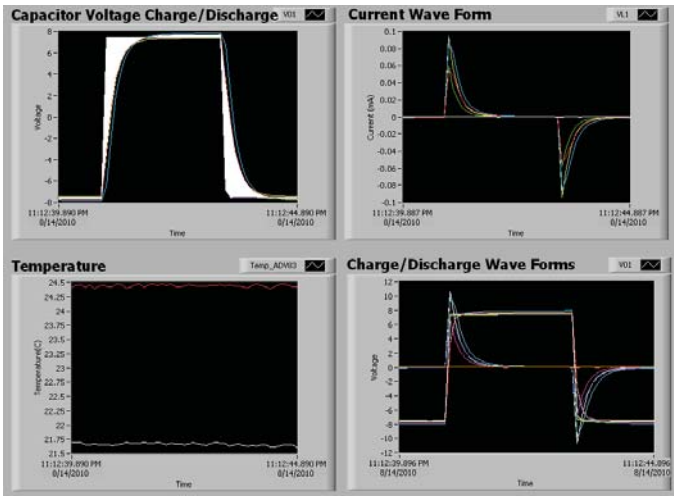

Fig. 10. Plots of the capacitor signals after 120 hours of experiment

TABLE I
AVERAGE INCREASE IN ESR

C/D (V)	Time (Hrs)	ESR(Ω)	ESR(Δ)	ESR/ Hr
Initial	0	0.0758	0	0
8	60	0.1074	3.16E-02	5.27E-05
8	15	0.1084	9.80E-04	6.53E-05
10	15	0.1098	1.44E-03	9.60E-05
10	15	0.1103	4.30E-04	2.87E-04
15	15	0.1145	4.37E-03	2.91E-04

TABLE II
AVERAGE DECREASE IN CAPACITANCE(C)

C/D (V)	Time (Hrs)	C(Ω)	C(Δ)	C/ Hr
Initial	0	1757	0	0
8	60	1705	5.20E-05	8.67E-07
8	15	1676	2.93E-05	1.96E-06
10	15	1647	2.83E-05	1.88E-06
10	15	1593	5.44E-05	3.63E-06
15	15	1547	5.64E-05	3.76E-06

voltage changes. It is observed that the rate of increase in the ESR is the maximum for the maximum stress voltage of 15V which is the maximum voltage applied to the capacitor for charging/discharging cycle.

Similar to the ESR discussed above we also observed the decrease in the capacitance of the electrolytic capacitors. The values were calculated from the measurements during the characterization of the capacitors. The details of the capacitance decrease are in table II. It is observed during the study that the rate of capacitance varies as the stressor voltage varies and is maximum when higher voltage is applied to the capacitor.

V. CONCLUSION

In the paper our main goal was to develop an experimental setup for monitoring the capacitor degradation under electrical stress. As discussed earlier the experimental setup for accelerated degradation was developed and implemented. The capacitors were subjected to varying electrical stressor conditions and their degradation rate was monitored. From the recorded data an initial analysis study was done. It is observed that the rate of degradation in the form of increase in ESR and decrease in capacitance varies as the stress voltage applied to the charge/discharge cycle.

In our future work we propose to degrade capacitors each on a separate hardware setup under different voltage conditions. Each set will consists of 6-8 capacitors which will be monitored using the data acquisition system and characterized using the EIS instrument at regular time intervals. The hardware for these setups in already developed and at present in the testing stage of the experiment cycle. As discussed earlier we are looking at four different voltage conditions for degradation, so in all we will have approximately 24-32 capacitors monitored at the same time. The data recorded from these experimental setups will give a good background on failure rates of the capacitors under voltage stress. This condition based monitoring data and can be used for our prognostic algorithms for calculating the RUL for other capacitors in different voltage operating conditions.

ACKNOWLEDGMENT

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